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EXAMINER
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ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/342,584	APPELT ET AL.	
	Examiner	Art Unit	
	Jose H Alcala	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-49* is/are pending in the application.

4a) Of the above claim(s) *11,16-18,24-36 and 39-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-15,19-23,37,38 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 6/29/99 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. **There are no copies in the file of any of the U.S. patents and the publications listed in the IDS.**

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 1/28/02 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance. However, the drawings have some other informalities as stated below:

3. Figures are improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "at least one

clearance between said electrically conductive circuitry and said plated through hole" must be shown or the feature(s) canceled from the claim(s). In the drawings the clearance is between the power plane and the through hole. In addition, the limitation that the plated through hole is electrically coupled to an electrically conductive circuitry, is not shown in the drawings. Furthermore the limitation that the dielectric layer is a resin coated copper foil is not in the drawings.No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 6 and 22 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear form the specification or the drawings, how can the dielectric layer be a resin-coated copper foil.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-8,10,12-15,19-23,37,38 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claims 1 and 48, it is not clear in lines 4-5, if the non-conductive layer is applied to the substrate layer or if it is the glass fibers that are applied to the substrate layer. For examination purposes it is interpreted as being the non-conductive layer the one applied to the substrate layer.

Regarding claims 6 and 22, it is not clear how the dielectric material can be a resin-coated copper foil. It is not clear how can copper be a dielectric material or part of a dielectric material.

Regarding Claim 8, it is not clear from the specification or the drawings how is the clearance located between the electrically conductive circuitry and the plated through hole, if the plated through hole extends through the electrically conductive circuitry.

Regarding Claim 10, it is unclear if the power plane is a different element than the conductive circuitry and where is the power plane located in relation to the other elements of the circuit board.

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: if the plated through hole also goes through the power plane or through the conductive circuitry.

Regarding Claim 13, the recitation: "said power plane is spaced from said through hole" is not clear. Is it that the plated through hole goes through the power plane or if the plated through hole is separated from the power plane. In addition, the claim recites the limitation "the space" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how can the non-conductive layer be positioned between said through hole and said electrically conductive circuit, if the plated through hole extends through the electrically conductive circuitry.

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: where is the clearance located in the electronic device package, and what is the location of the clearance in relation to the other elements of the package.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-8, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pellegrino (US Patent No. 4,521,262) in view of Day et al. (US Patent No. 5,026,624). As best understood by the examiner:

Regarding Claim 1, Pellegrino teaches a printed circuit board comprising: a substrate layer (Reference number 48) comprising impregnated glass fibers; a non-conductive layer (Reference number 40) comprising a dielectric material; and an electrically conductive circuitry (Reference number 44) comprising a conductive material formed on said non-conductive layer such that said non-conductive layer lies between said substrate layer and said conductive material.

The recitations: "for use in an electronic device package" and "to prevent shorts there between caused by migration of said conductive material along said glass fibers" are intended use limitations, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Pellegrino fails to teach that the non-conductive layer is "free of continuous glass fibers". Day teaches an epoxy based dielectric material that is free of continous glass

fibers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Pellegrino and Day in order to have the non-conductive layer be made of a dielectric material free of continuous glass fibers, thus making the board be fire and flame retardant, and reducing the thickness of the layers, improving integration and the dimensional control of the fabricating process.

Regarding Claim 2, Pellegrino teaches a plated through hole (Reference number 54, plated with Reference numbers 56 and 58) extending through said substrate layer and said non-conductive layer and electrically coupled to said circuitry.

Regarding Claim 3, the combination of Pellegrino and Day as stated for claim 1, teaches that the dielectric material comprises a photoimageable dielectric material (Day reference, column 2, lines17-20).

Regarding Claims 4 and 5, Pellegrino as modified by Day fails to explicitly teach that the dielectric material comprises a polyimide, a Kevlar-based paper impregnated with epoxy resin. The use of a polyimide and Kevlar-based paper impregnated with epoxy resin, as dielectric material of a printed circuit board is well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention, to use any of these two materials as the material of the dielectric, to achieve the desired dielectric characteristic for the printed circuit board. In addition it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 6, Pellegrino teaches that the dielectric material is a resin (Reference number 40) coating a copper foil (Reference number 44).

Regarding Claim 7, Pellegrino teaches that said substrate layer is prepreg comprising a glass fabric impregnated with epoxy resin (Column 4, lines 60-63).

Regarding Claim 8, Pellegrino teaches at least one clearance (Reference number 52) between said electrically conductive circuitry and said plated through hole filled with said dielectric material.

Regarding Claim 37, Pellegrino as modified by Day, fails to explicitly teach that the thickness of said non-conductive layer is between 0.5 mils and 5 mils, but it is suggested that the thickness of the substrate will vary depending upon the specific intended purpose for the circuit board (Column 3, lines 47-49 of Pellegrino). It would have been obvious to one of ordinary skill in the art at the time the invention was made to change the thickness of the non-conductive layer in order to make the printed board more or less rigid. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See In re Aller, 105 USPQ 233.

11. Claims 1-8, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffarth et al. (US Patent NO. 4,868,350). As best understood by the examiner:

Regarding Claim 1, Hoffarth et al. teaches a printed circuit board comprising: a substrate layer (the dielectric layer that is at the bottom of the lower core 20, as seen in figure 4); a non-conductive layer (Reference number 11 a-d) comprising a dielectric

material free of continuous glass fibers applied to said substrate layer; and an electrically conductive circuitry (Reference number 19) comprising a conductive material formed on said conductive layer such that said non-conductive layer lies between said substrate layer and said electrically conductive material

The recitation "for use in an electronic device package" is merely a label for the intended use of the printed circuit board, as well as the recitation: "to prevent shorts therebetween caused by migration of said electrically conductive circuit along said glass fibers", and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Hoffarth fails to explicitly teach that the substrate layer comprises impregnated glass fibers, but suggests that the encapsulant can be made comprising impregnated glass fibers (column 2, lines 50-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hoffarth to make the substrate comprising impregnated glass fibers, in order to increase the thickness of the layers and in that way increasing the firmness of the circuit board.

Regarding Claim 2, Hoffarth teaches at least one plated through hole (Reference number 15) extending through said substrate layer and said non-conductive layer and electrically coupled to said circuitry.

Regarding Claims 3, 4 and 5, Hoffarth fails to explicitly teach that the dielectric material comprises a photoimageable dielectric material, a polyimide, a Kevlar-based

paper impregnated with epoxy resin. The use of a polyimide and Kevlar-based paper impregnated with epoxy resin, as dielectric material of a printed circuit board is well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention, to use any of these two materials as the material of the dielectric, to achieve the desired dielectric characteristic for the printed circuit board. In addition it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 6, Hoffarth fails to teach that the dielectric material comprises resin-coated copper foil. It is well known in the art to insert metallic materials on a dielectric material to improve its conductivity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a copper foil and coat it with resin in order to improve conductivity of the dielectric material.

Regarding Claim 7, Hoffarth suggests that the substrate layer is glass fabric impregnated with epoxy resin, the fact that it is a prepeg is a product by process limitation.If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re

Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding Claim 8, Hoffarth teaches at least one clearance (See the space marked with reference letter D in Figure 1) between said electrically conductive circuitry and said plated through hole filled with said dielectric material.

Regarding Claim 37, Hoffart fails to explicitly teach that the thickness of said non-conductive layer is between 0.5 mils and 5 mils, but it is suggested that if the thickness of the substrate is reduced, the dimensional control of the fabricating process is improved (column 4, lines 34-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to change the thickness of the non-conductive layer in order to make the printed board more or less rigid, and to reduce the thickness inorder to improve the dimensional control of the fabrication process. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See In re Aller, 105 USPQ 233.

12. Claims 10,12,13,14,15,19,20,21,22,23,38 and 48 rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffarth et al. (US Patent NO. 4,868,350). As best understood by the examiner:

Regarding Claim 48, Hoffarth et al. teaches a printed circuit board comprising: a substrate (the dielectric layer that is at the bottom of the lower core 20, as seen in figure 4); an electrically conductive circuit (Reference number 19); and a non-conductive layer (Reference number 11 a-d) free of continuous glass fibers comprising a dielectric material applied to said substrate such that said non-conductive layer lies between said substrate and said electrically conductive circuit to prevent shorts there between caused by migration of said electrically conductive circuit along said glass fibers.

The recitation "an electronic device package" is merely a label for the intended use of the printed circuit board, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Hoffarth fails to explicitly teach that the substrate comprises impregnated glass fibers, but suggests that the encapsulant can be made comprising impregnated glass fibers (column 2, lines 50-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hoffarth to make the substrate comprising impregnated glass fibers, in order to increase the thickness of the layers and in that way increasing the firmness of the circuit board.

Regarding Claim 10, Hoffarth teaches at least one power plane (Reference number 13).

Regarding Claim 12, Hoffarth teaches at least one plated through hole (Reference number 15) extending through said substrate and said non-conductive layer.

Regarding Claim 13, Hoffarth teaches that said power plane (Reference number 13) is spaced from said through hole (See figure 4) and said board includes a non-conductive layer comprising a dielectric material free of continuous glass fibers in the space between said power plane and said through hole. The recitation "to prevent a short there between" is merely an intended use of the non-conductive layer, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 14, Hoffarth teaches the non-conductive layer is positioned between said through hole and said electrically conductive circuit (See figure 14).

Regarding Claim 15, Hoffarth teaches at least one clearance filled with said dielectric material (See the space marked with reference letter D in Figure 1).

Regarding Claims 19, 20 and 21, Hoffarth fails to explicitly teach that the dielectric material comprises a photoimageable dielectric material, a polyimide, a Kevlar-based paper impregnated with epoxy resin. The use of a polyimide and Kevlar-based paper impregnated with epoxy resin, as dielectric material of a printed circuit board is well known in the art. It would have been obvious to one of ordinary skill in the

art at the time of the invention, to use any of these two materials as the material of the dielectric, to achieve the desired dielectric characteristic for the printed circuit board. In addition it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 22, Hoffarth fails to teach that the dielectric material comprises resin-coated copper foil. It is well known in the art to insert metallic materials on a dielectric material to improve its conductivity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a copper foil and coat it with resin in order to improve conductivity of the dielectric material.

Regarding Claim 23, Hoffarth suggests that the substrate layer is glass fabric impregnated with epoxy resin, the fact that it is a prepeg is a product by process limitation.If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new

method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding Claim 38, Hoffarth fails to explicitly teach that the thickness of said non-conductive layer is between 0.5 mils and 5 mils, but it is suggested that if the thickness of the substrate is reduced, the dimensional control of the fabricating process is improved (column 4, lines 34-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to change the thickness of the non-conductive layer in order to make the printed board more or less rigid, and to reduce the thickness inorder to improve the dimensional control of the fabrication process. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See In re Aller, 105 USPQ 233.

Response to Arguments

13. Applicant's arguments with respect to claims 1-8,10,12-15,19-23,37,38 and 48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention: Kerrick (US Patent No. 5,763,060), Appelt et al. (US Patent No. 5,981,880), Kambe et al. (US Patent No. 6,323,439), Endoh et al. (US Patent No. 5,374,788) and Fasano et al. (US Patent No. 5,949,030).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
May 14, 2002

KAMAND CUNEO
PRIMARY EXAMINER